WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an insulator;

a semiconductor fin formed on the insulator;

a source region adjacent a first end of the fin formed on the insulator;

a drain region adjacent a second end of the fin formed on the insulator;

a first sidewall spacer formed adjacent a first side of the fin, the first sidewall spacer having a substantially triangular shaped cross-section;

a second sidewall spacer formed adjacent a second side of the fin, the second sidewall spacer having a substantially triangular shaped cross-section; and

a gate formed over the fin and the first and second sidewall spacers in a channel region of the semiconductor device.

2. The semiconductor device of claim 1, wherein the first and second sidewall spacers cause a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers.

3. The semiconductor device of claim 1, wherein the first and second sidewall spacers slope away from the fin.

4. The semiconductor device of claim 1, wherein the gate includes an electrode portion formed away from the fin.

5. The semiconductor device of claim 1, wherein the first and second sidewall spacers are formed to a width ranging from about 150 Å to about 1000 Å.

6. The semiconductor device of claim 1, wherein the first and second sidewall spacers are formed of polysilicon.

7. The semiconductor device of claim 6, wherein the gate comprises polysilicon.

8. A method of manufacturing a semiconductor device, the method comprising:

forming a fin structure on an insulator;

forming a first sidewall spacer adjacent a first side of the fin structure, the first sidewall spacer having a substantially triangular shaped cross-section;

forming a second sidewall spacer adjacent a second side of the fin structure, the second sidewall spacer having a substantially triangular shaped cross-section;

depositing a gate material layer over the fin structure, the first sidewall spacer, and the second sidewall spacer, the first and second sidewall spacers causing a gradual sloping of the gate material layer over the fin and the first and second sidewall spacers; and

etching the gate material layer to form at least one gate for the semiconductor device.

9. The method of claim 8, wherein the gradual sloping of the gate material layer reduces micromasking effects during the etching of the gate material layer.

10. The method of claim 8, further comprising:

forming a source region at a first end of the fin structure.

11. The method of claim 10, further comprising:

forming a drain region at a second end of the fin structure.

12. The method of claim 8, wherein the first and second sidewall spacers comprise polysilicon.

13. The method of claim 8, wherein the gate material layer includes an electrode portion formed away from the fin.

14. The method of claim 8, wherein the first and second sidewall spacers are formed to a width of about 150 Å to about 1000 Å.

15. The method of claim 8, wherein the gate material layer comprises polysilicon.

16. A FinFET device comprising:

an insulator;

a semiconductor fin formed on the insulator;

a source region connected to a first end of the fin and formed on the insulator;

a drain region connected to a second end of the fin and formed on the insulator;

a first sidewall spacer formed adjacent a first side of the fin in a roughly triangular shape;

a second sidewall spacer formed adjacent a second side of the fin in a roughly triangular shape; and

a gate material layer formed over the fin, the first sidewall spacer, and the second sidewall spacer in a direction perpendicular to a direction of the fin, whereby the first and second sidewall spacers cause a topology of the gate material layer to smoothly transition over the fin and the first and second sidewall spacers.

17. The FinFET device of claim 16, wherein the first and second sidewall spacers are formed to a width of about 150 Å to about 1000 Å.

18. The FinFET device of claim 16, wherein the first and second sidewall spacers slope away from the fin.

19. The FinFET device of claim 18, wherein the first and second sidewall spacers reduce micromasking effects during etching of a gate material to form the gate.